COA Virtual LAB adapted for web based usage

1. Overview

Web Based Virtual Lab (WBVL) so far developed is ready to perform any experiment with combinational logic. User needs to add necessary logic GATEs, connections and bit-switches (to represent inputs and outputs) in the circuit and then click 'Simulate' button. The facility to simulate sequential circuit is in progress.

2. Technical Insight

The Virtual Lab has been developed using HTML 5 CANVAS and JavaScript. Two overlaid canvases have been used to provide the main framework of the simulator. The bottom layer canvas is mainly generating the breadboard. The top layer is generating the circuit. The circuit needs to be redrawn every time a new element is added/deleted or state of the circuit is changed. But the breadboard part remains intact throughout the experiment. This design strategy provides a faster response with even a complex circuit.

3. Manual

A breadboard like panel is given with dotted horizontal and vertical lines to draw the digital circuit. The elements for the digital circuit is provided at the right hand side of the panel under the 'Inputs-Outputs' section and the 'Logic Gates' section. Any element could be added to the circuit by single clicking on the element and dragging it to the right position on the panel. BITSwitch element is for providing true-false input to the circuit from external source. The BITDisplay element is to provide the final true-false output from the circuit. A connection between elements could be done by left click the mouse at the source position and then hold the click and drag it to the destination position and then release the click. The connection could be drawn either vertically or horizontally on the dots. Hence to draw a connection with vertical and horizontal lines, multiple horizontal and vertical lines need to be drawn separately. To delete an element or connection, double click on the element or connection and then click the delete button.

To simulate the circuit, just click the simulate button given at the right side of the panel under the 'Action' section.

4. Sample Experiments

1. 2 input multiplexer (MUX)

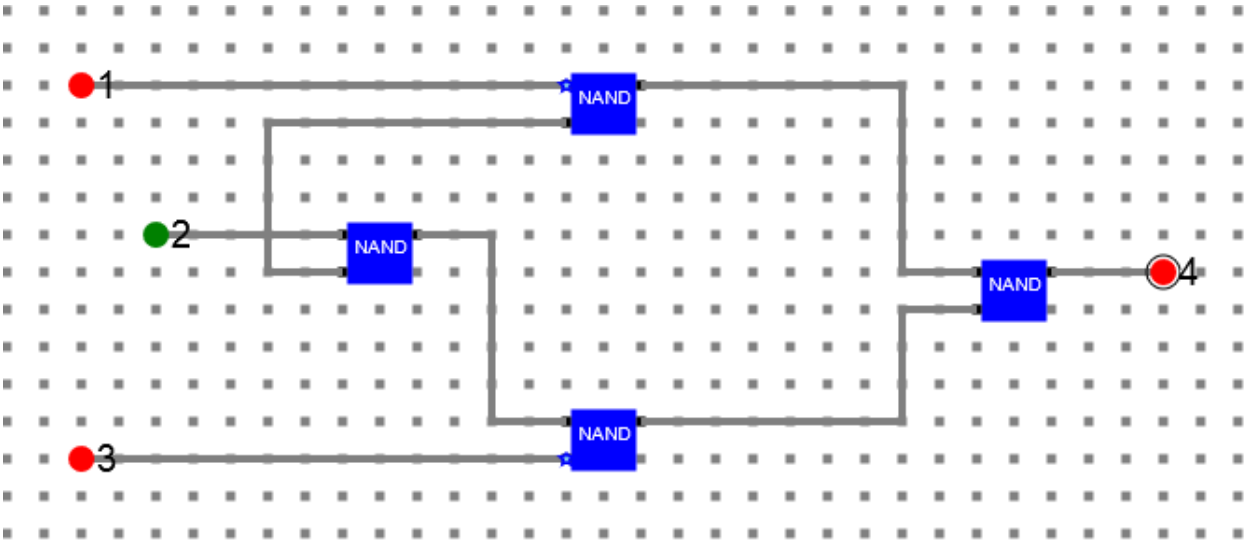
Truth Table

	input-1	Input-2	Control Switch	Output
Case 1	0	0	1	0
Case 2	0	1	1	0
Case 3	1	0	1	1
Case 4	1	1	1	1
Case 5	0	0	0	0
Case 6	0	1	0	1
Case 7	1	0	0	0
Case 8	1	1	0	1

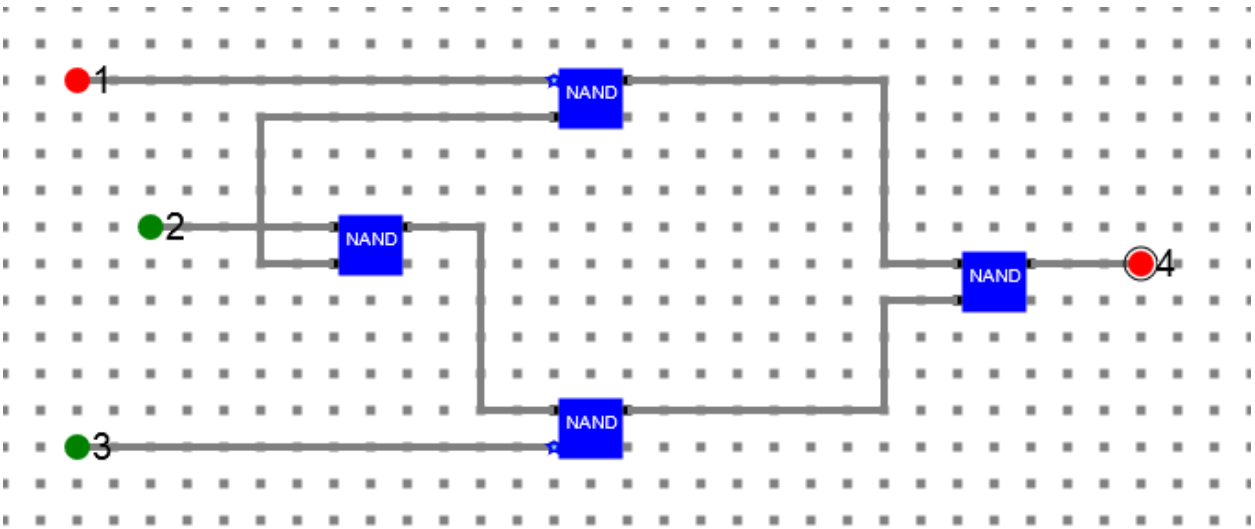
A 2 input multiplexer has been designed and simulated as below using all NAND Gates. (Green-1, RED-0)

Input-1: Bit-1
Input-2: Bit-3
Control Switch: Bit-2
Output: Bit-4

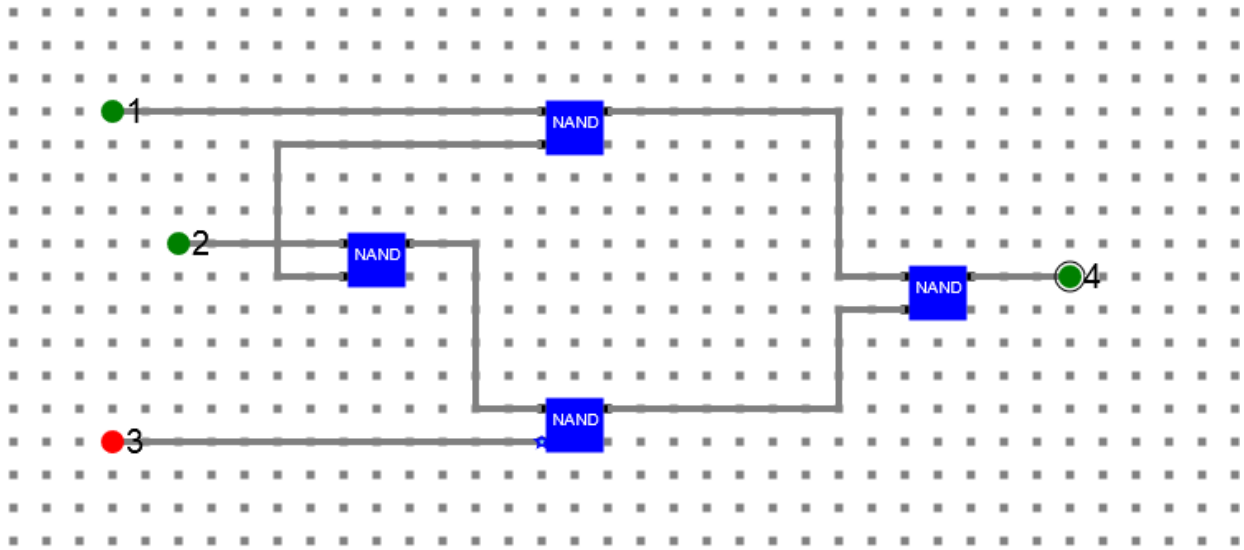
Case 1:



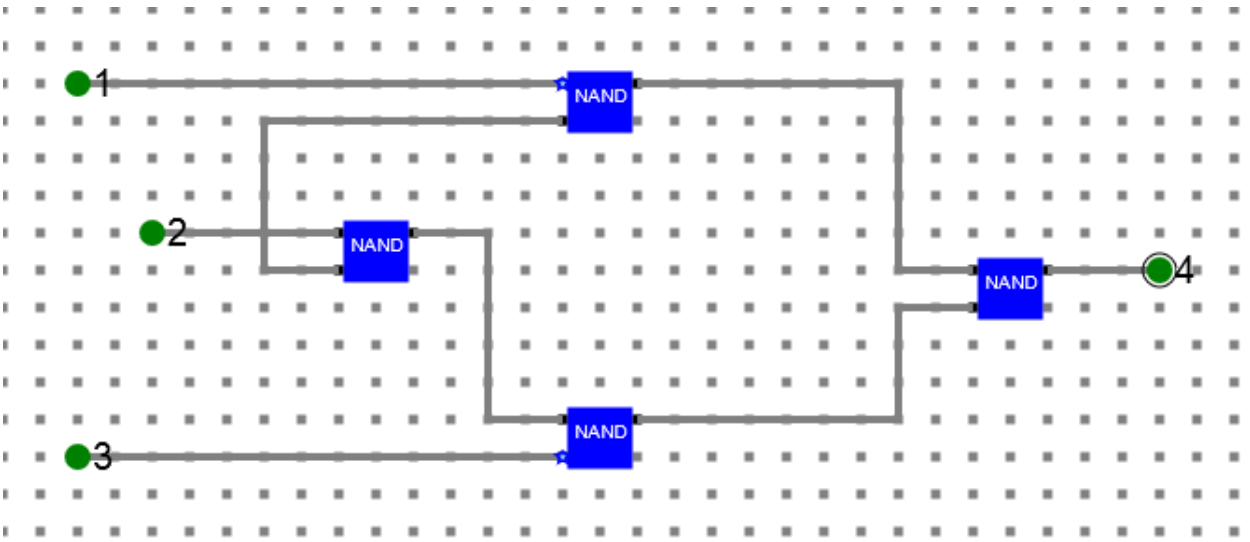
Case 2:



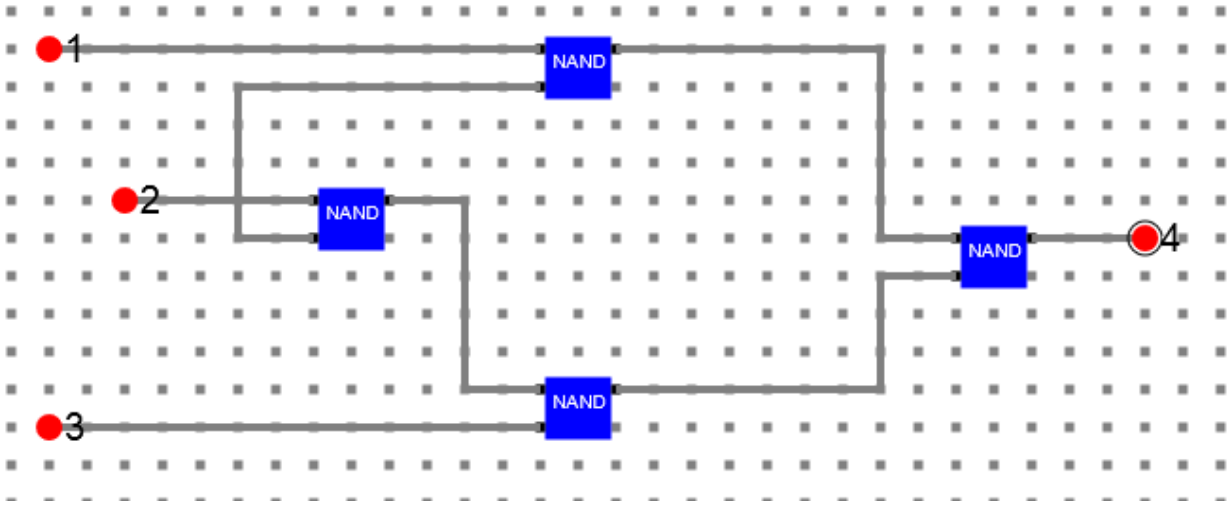
Case 3:



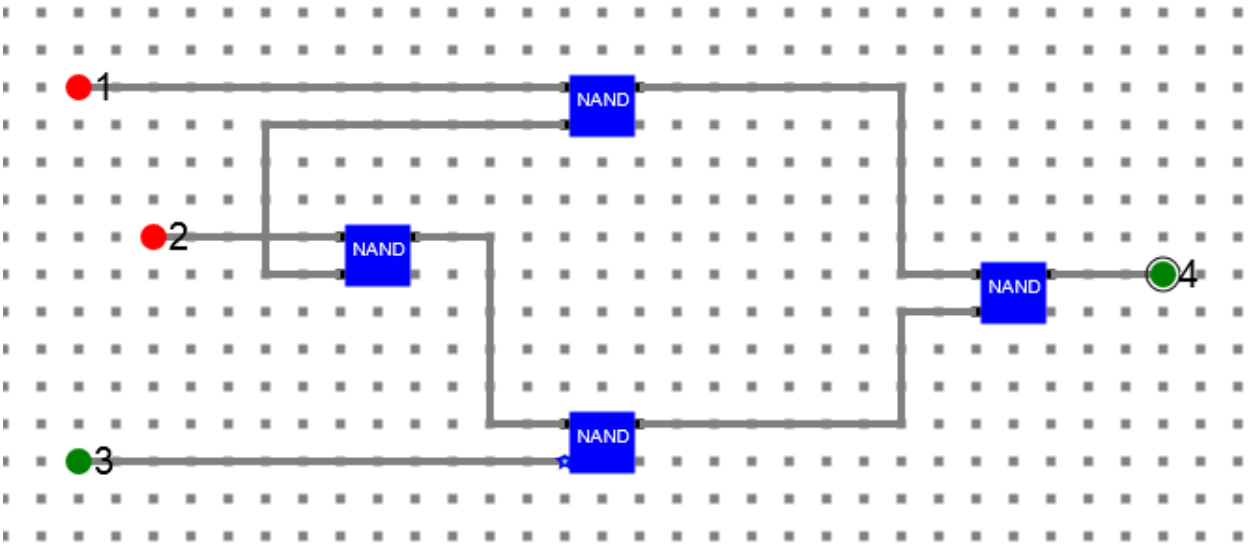
Case 4:



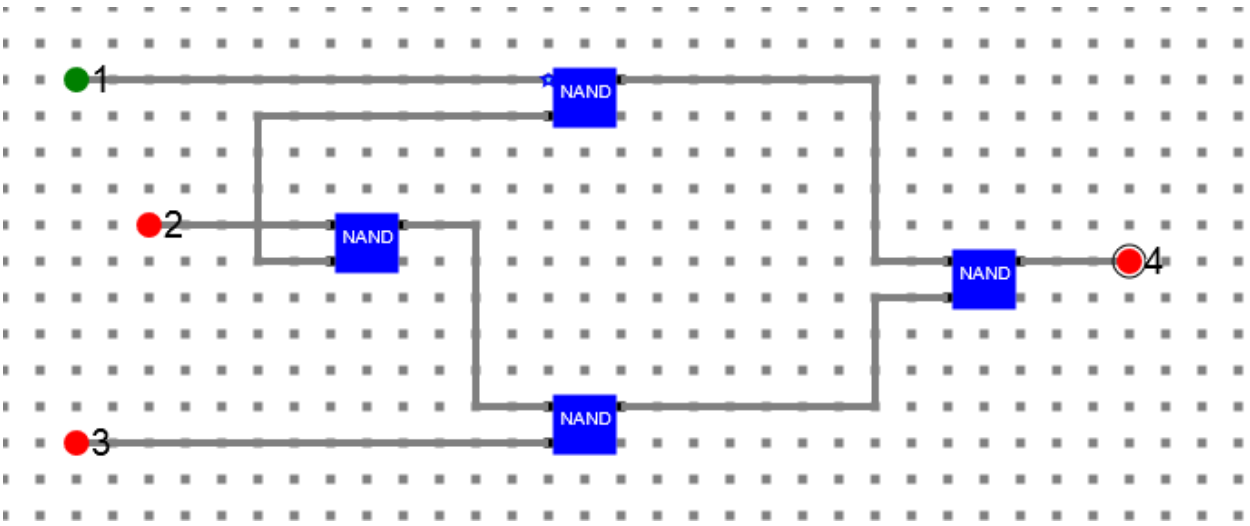
Case 5:



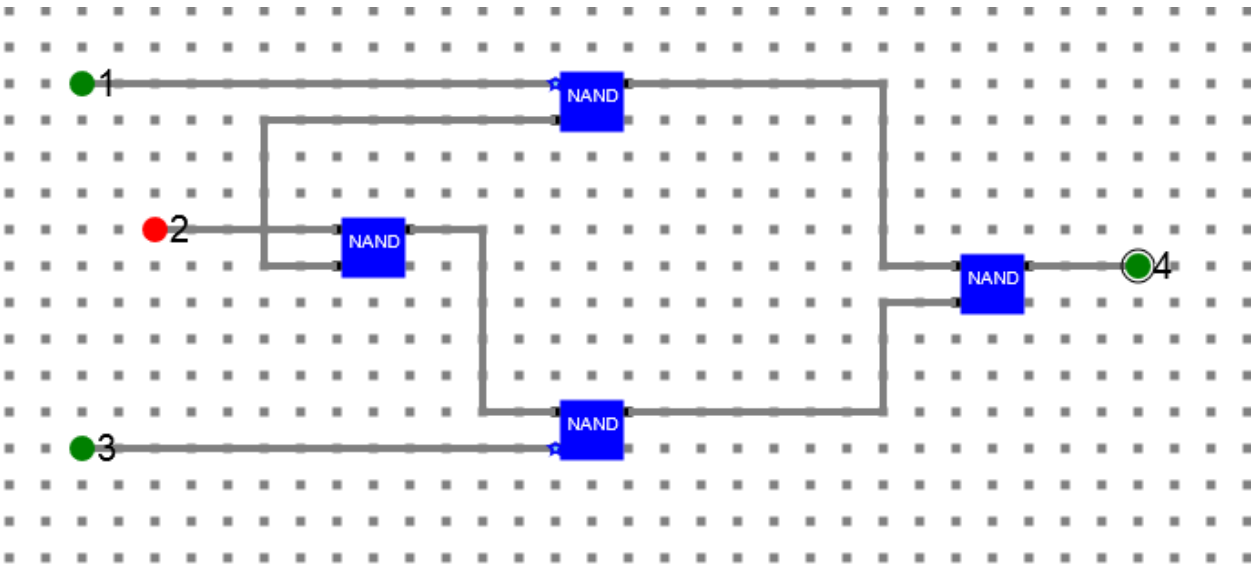
Case 6:



Case 7:



Case 8:



2. Half Adder

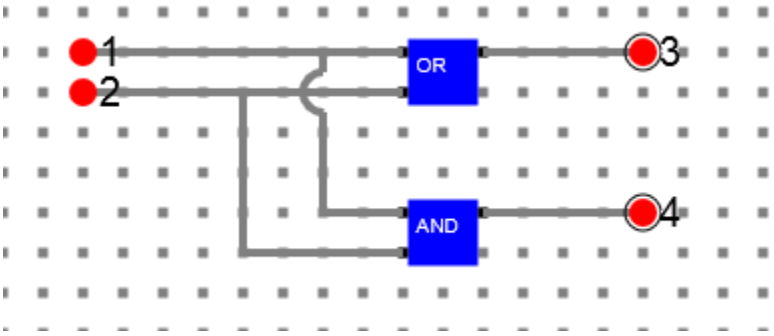
Truth Table

	Inputs		Output	
	A	B	S	C
Case-1	0	0	0	0
Case-2	0	1	1	0
Case-3	1	0	1	0
Case-4	1	1	0	1

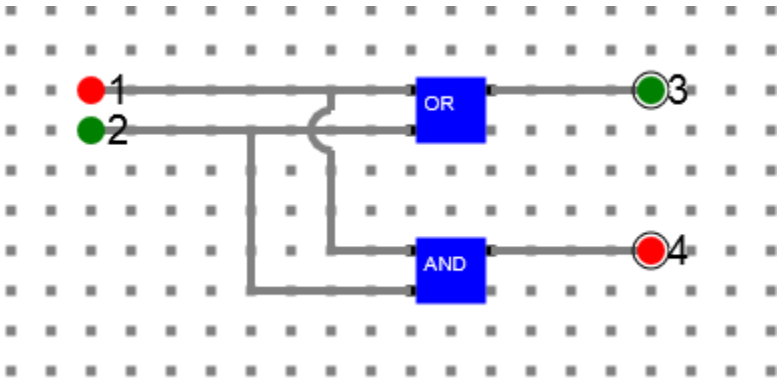
A half adder has been designed and simulated as below. (Green-1, RED-0)

A: Bit-1
B: Bit-2
S: Bit-3
C: Bit-4

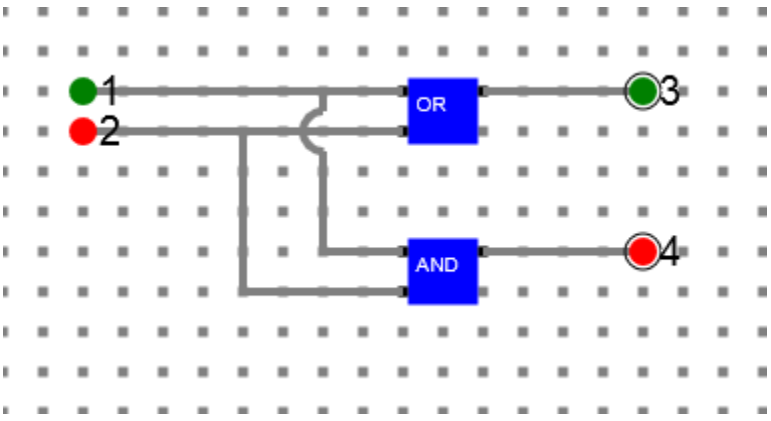
Case 1:



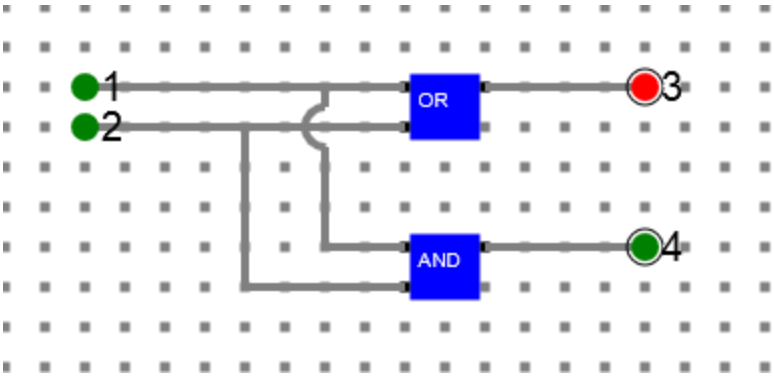
Case 2:



Case 3:



Case 4:



5. Conclusion

With the current development of the Virtual Lab any complex combinational logic could be simulated. The work is in progress to include facility to simulate any complex sequential logic as well. Once it is ready, user would be able to develop circuit which could be converted into a component. Then the component could be used in any other circuit as a new IC.